## Remarks

In the Office Action of April 5, 2005, the Examiner restricted examination to the claims of one of Group I (claims 1-6 and 15-18) and Group II (claims 7-14); objected to the specification based on an informality; rejected claims 1-6 and 15-18 under 35 U.S.C. § 102(b) based on U.S. Patent No. 6,395,589 to Yu ("Yu"); rejected claims 1, 2, 4-6 and 18 under 35 U.S.C. § 102(e) based on U.S. Patent Publication 2004/0227187 to Cheng et al. ("Cheng"); and rejected claims 3 and 15-17 under 35 U.S.C. § 103(a) based on Cheng and further in view of U.S. Patent No. 6,455,383 to Wu ("Wu").

Applicants confirm the election of the claims in Group I (claims 1-6 and 15-18) for examination.

By this Amendment, Applicants have amended the specification to correct a typographical error and amended claims 1 and 18 to improve form and, in the case of claim 1, to substantially incorporate the features of claim 3. Claims 3 and 7-14 have been canceled without prejudice or disclaimer.

Claims 1-6 and 15-18 stand rejected under 35 U.S.C. § 102(b) based on Yu. Applicants respectfully traverse this rejection.

Claim 1, as amended, is directed to a semiconductor FinFET device comprising an insulator; a semiconductor layer formed on the insulator, the semiconductor layer including a fin portion corresponding to a channel of the

semiconductor device; a source region formed at a first end of the semiconductor layer, a height of the source region being higher than that of the fin; a drain region formed at a second end of the semiconductor layer, a height of the drain region being higher than that of the fin; a metal gate region formed to overlap at a top surface and at least one side surface of the fin; and oxide sidewalls formed adjacent to the metal gate region and above the top surface of the fin.

Applicants submit that Yu does not disclose or suggest a number of the features recited in amended claim 1. For example, Yu does not disclose or suggest a "fin portion corresponding to a channel of the semiconductor device," as recited in claim 1. A "fin," as described in the specification and as is well known in the art, refers to a vertical conducting channel in a FinFET type of MOSFET (see, for example, the pending specification, paragraph 0026). Yu does not disclose the fin portion corresponding to a channel of a semiconductor device, as recited in claim 1. Yu is directed to the fabrication of a fully depleted field effect transistor. (Yu, Title). The transistor of Yu is not a FinFET. Instead, the channel region of Yu, as with a traditional MOSFET, appears to be located entirely below the gate structure of the MOSFET. This can be clearly seen in Fig. 17 of Yu, in which gate structure 246 is positioned above a thin silicon channel region.

Claim 1 further recites a metal gate region formed to overlap at a top surface and at least one side surface of the fin. As mentioned, Yu does not

disclose a fin. Further, even if the channel region below gate structure 246 was somehow construed to correspond to a fin, the gate structure 246 of Yu does not overlap at a top surface and at least one side surface of the fin. Instead, gate structure 246 appears to only cover a top surface of the underlying channel area.

Still further, claim 1, as amended, recites oxide sidewalls formed adjacent the metal gate region and above the top surface of the fin. Applicants submit that Yu completely fails to disclose or suggest any such sidewalls.

For at least these reasons, Applicants submit that Yu does not disclose many of the features recited in claim 1. Accordingly, the rejection of claim 1 based on Yu is improper and should be withdrawn. The rejection of claims 2-6 based on Yu are also improper and should be withdrawn, at least by virtue of the dependency of these claims from claim 1.

Independent claim 15 and its dependent claims 16-18 were also rejected under 35 U.S.C. § 102(b) based on Yu. Claim 15 includes a number of features similar to those in claim 1. Accordingly, for reasons similar to those given above with regard to claim 1, Applicants submit that the rejection of claim 15 based on Yu is also improper and should be withdrawn. Claims 16-18 depend from claim 15 and the rejections of these claims are also improper and should be withdrawn.

Independent claim 1 and dependent claims 2, 4-6, and 18 stand rejected under 35 U.S.C. § 102(e) based on Cheng. Claim 1, as amended, recites a feature similar to that previously recited in independent claim 3. In particular,

claim 1, as amended, is directed to a FinFET device including a metal gate region and oxide sidewalls formed adjacent to the metal gate region and above the top surface of the fin. Applicants submit that Cheng does not disclose or suggest this feature of amended claim 1. The Examiner concedes this point at page 8 of the Office Action. Accordingly, the rejections of claim 1 and its dependent claims 2 and 4-6 based on Cheng should be withdrawn. Claim 18 has been amended to depend from claim 15 and, therefore, the rejection of this claim is addressed below.

Claims 3 and 15-17 stand rejected under 35 U.S.C. § 103(a) as being obvious in view of Cheng and Wu. Applicants respectfully traverse this rejection.

As mentioned, amended claim 1 includes features similar to those previously recited in claim 3. Accordingly, Applicants will assume that the previous rejection of claim 3 now applies to claim 1. In this rejection, the Examiner contends that Cheng discloses many of the features recited in claims 1 and 3, but concedes that Cheng does not disclose oxide sidewalls formed adjacent to a metal gate region. (Office Action, page 8). The Examiner relies on Wu to disclose sidewall spacers, and contends that one of ordinary skill in the art would have found it obvious to modify Cheng to include the sidewall spacers of Wu "in order to provide protection to the gate from external effects and from short circuit to the source/drain contacts." (Office Action, page 9).

Wu is directed to methods for manufacturing scaled MOSFETs. (Wu,

Title). The MOSFETs of Wu are not FinFETs. Instead, as is shown, for example, in Fig. 2A of Wu, a MOSFET includes an oxide 310a formed under a stacked gate. The channel area in this MOSFET is below the oxide/stacked gate area. Accordingly, the MOSFET of Wu is a standard MOSFET and is not a FinFET.

In this regard, Applicants disagree with the Examiners assertion that Wu discloses many of the features recited in amended claim 1 (see Office Action, first paragraph of page 9, which cites Figs. 1 and 2 of Wu). Applicants strongly disagree with the Examiner's interpretation of Wu.

The Examiner states that Wu discloses a fin "under the gate structure 102a." (Office Action, page 9). Applicants submit that although Wu discloses a channel for a MOSFET under gate structure 102a, the channel cannot be said to correspond to "a fin portion corresponding to a channel of the semiconductor device" of the FinFET device recited in claim 1. As mentioned previously, a fin in a FinFET refers to a vertical conducting channel. Wu, however, discloses a standard MOSFET having a horizontal channel.

The Examiner further states, at page 9 of the Office Action, that metal gate region 102a of Wu corresponds to the metal gate region recited in claim 1, which is formed to overlap at a top surface and at least one side surface of the fin. Again, Applicants respectfully disagree with the Examiner's interpretation of Wu. Metal gate region 102a of Wu, as is clearly shown in Fig. 1A, if formed above the

channel region of the MOSFET, but cannot be said to overlap, as is recited in claim 1, at a top surface and at least one side surface of the fin.

Accordingly, contrary to the Examiner's allegations, Applicants submit that Wu does not disclose many of the features recited in claim 1.

Additionally, Applicants submit that the Examiner has not made a proper *prima facie* case of obviousness with regard to Cheng and Wu. The basic criteria for establishing a *prima facie* case of obviousness are articulated in M.P.E.P. § 2142. One of these criterion is that there must be some suggestion or motivation, either in the reference(s) themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. A second of these criterion is that there must be a reasonable expectation of success. Applicants submit that the Examiner has not shown proper motivation to combine Cheng and Wu in the manner suggested.

The Examiner relies on Wu for the oxide sidewall spacers recited in amended claim 1, and states that it would have been obvious to modify Cheng in view of Wu "in order to provide protection to the gate from external effects and from short circuit to the source/drain contacts." (Office Action, page 9). Applicants respectfully disagree with the Examiner's conclusion of obviousness. Cheng discloses a multi-gate FinFET device. (Cheng, paragraphs 0032 and 0033). Wu, as discussed above, discloses a more conventional FET device. Applicants submit that these two structures would be recognized by one of

ordinary skill in the art as different types of semiconductor FET structures and that specific parameters or features (such as sidewall spacers) in one device could not simply be applied to the other device. Accordingly, one of ordinary skill in the art reading Wu would not be motivated to simply add a spacer from the FET device of Wu to the FinFET device of Cheng. Thus, Applicants submit that the Examiner has not made a prima facie case of obviousness with regard to Cheng and Wu.

For at least these reasons, Applicants submit that a rejection based on Cheng and Wu under 35 U.S.C. § 103(a) of claim 1 is not proper. Claims 2-6, at least by virtue of their dependency from claim 1, are also patentable in view of Cheng and Wu.

Claims 2-6 individually recite features that are not disclosed or suggested by Cheng and Wu, either alone or in combination. Claim 5, for example, further defines the features of claim 1 and recites that "a distance between the insulator and the metal gate region is about 500 Å to about 700 Å and a distance between the insulator and a top of the source or the drain region is about 600 Å to about 1000 Å." The Examiner contends that Cheng discloses these features and points to paragraph 0042 and page 6, claim 24. (Office Action, page 7). These sections of Cheng, however, in no way disclose or suggest the specific feature size ranges recited in claim 5. Paragraph 0042 of Cheng generally discloses that fin-channel 104 "typically has small heights." Claim 24 of Cheng states that

"each of said fin-shaped strips comprises a width and a height ranging between 1 nm and 200 nm." These sections of Cheng relate to the dimensions of the fins disclosed by Cheng, but do not disclose or suggest the ranges recited in claim 5, which relate to a distance between the insulator and the metal gate region and to a distance between the insulator and a top of the source or the drain region. Thus, Cheng does not disclose or suggest the features of claim 5.

Independent claim 15 and its dependent claims 16 and 17 were also rejected by the Examiner under 35 U.S.C. § 103(a) based on Cheng and Wu. Additionally, claim 18, as amended, now depends from claim 15.

Independent claim 15 is directed to a FinFET device comprising an insulator; a semiconductor layer formed on the insulator, the semiconductor layer including a fin portion corresponding to a channel of the semiconductor device; a source region formed from a first end of the semiconductor layer, a height of the source region being higher than that of the fin and a width of the source region being wider than that of the fin; and a drain region formed from a second end of the semiconductor layer, a height of the drain region being higher than that of the fin and a width of the drain region being wider than that of the fin. Claim 15 further recites a metal gate region formed to overlap at a top surface and at least one side surface of the fin and sidewalls spacers formed adjacent at least portions of the metal gate region.

Applicants submit, based on reasons similar to those given above with

regard to claim 1, that Cheng and Wu, either alone or in combination, fail to disclose each of the features recited in claim 15. Accordingly, the rejection of this claim should be withdrawn. The rejection of dependent claims 16-18 should also be withdrawn, at least by virtue of their dependency from claim 15.

Claims 16-18 individually recite features that are not disclosed or suggested by Cheng and Wu, either alone or in combination. Claim 16, for example, depends from claim 1 and recites that the sidewall spacers have a width ranging from about 150 Å to about 1000 Å. In rejecting claim 16, the Examiner points to column 4, lines 58-60 of the "Cheng/Shih" reference. (Office Action, page 11). Applicants request clarification as to what reference the Examiner is referring to by the "Shih" reference. Shih is not of record in this application. Additionally, column 4, lines 58-60 of Wu do not mention sidewall spacers or give dimensions of semiconductor device features. In any event, Applicants submit that Cheng and Wu, either alone or in combination, do not disclose or suggest the range recited in claim 16.

Claim 18, as amended, further defines the features of claim 15 and recites that "a thickness of the fin portion ranges from about 500 Å to about 700 Å and a thickness of the source and drain regions ranges from about 600 Å to about 1000 Å." In rejecting this claim, the Examiner points to paragraph 0042 and claim 24 of Cheng as allegedly disclosing the features recited in this claim. (Office Action, page 8). These sections of Cheng relate to the dimensions of the fins disclosed

by Cheng, but in no way disclose or suggest the ranges recited in claim 18, which include a thickness of the source and drain regions ranges from about 600 Å to about 1000 Å. Thus, Cheng and Wu do not disclose or suggest the features of claim 18.

Newly added claim 19 depends from claim 1 and recites that the sidewall spacers have a width ranging from about 150 Å to about 1000 Å. Applicants submit that this feature is not disclosed or suggested by the prior art of record.

In view of the foregoing amendments and remarks, Applicants respectfully request withdrawal of the outstanding rejections and the timely allowance of this application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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